

Variant 005 (fully populated) shown. For block diagrams of other Variants, refer to the TIDA-01480 Design Guide (TIDUDN1)

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	2017-11-14	Brian Berner	1st Build
E2	N/A	2017-12-06	Brian Berner	1st Web Release

A

B

C

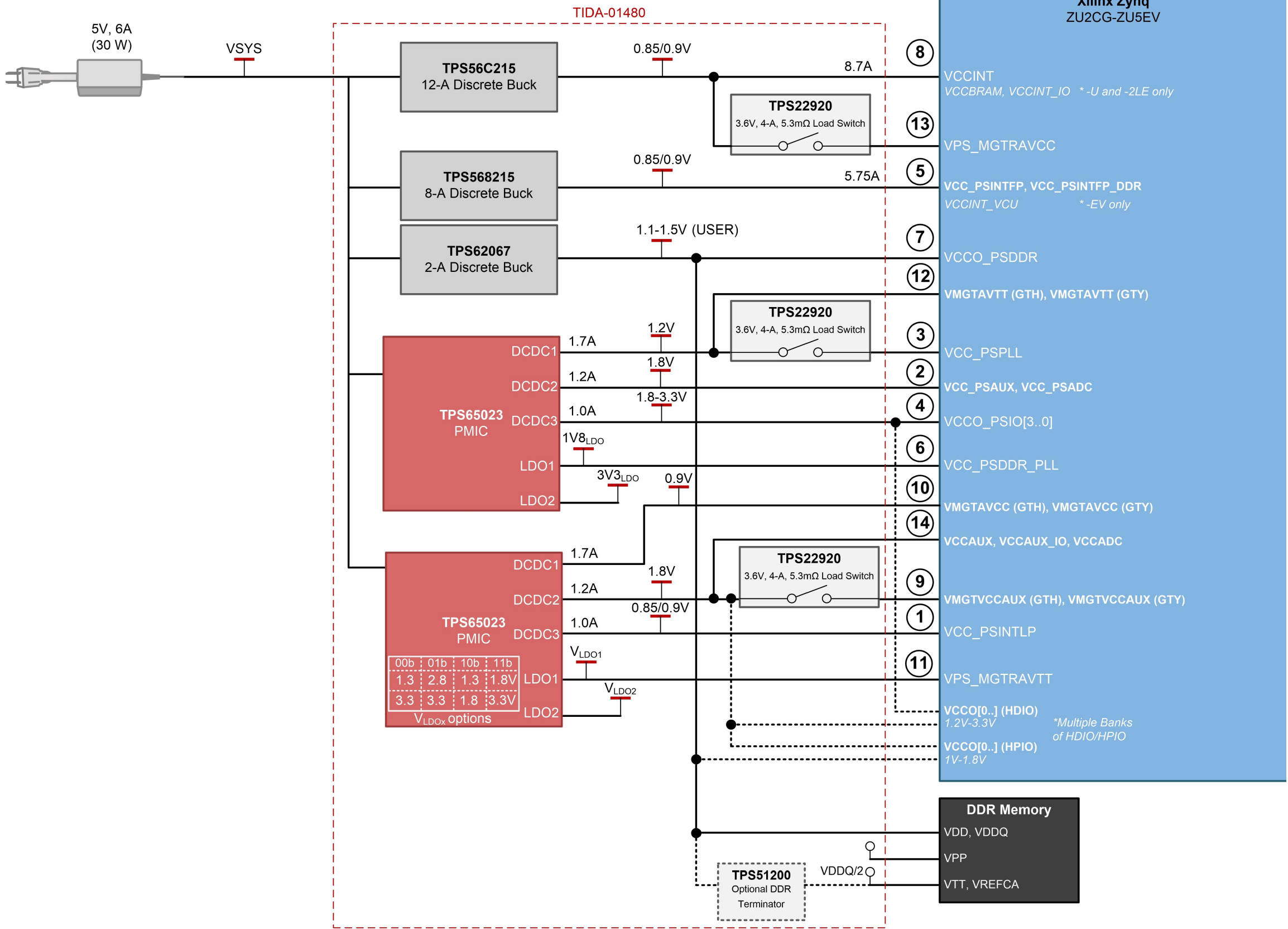
D

A

B


C

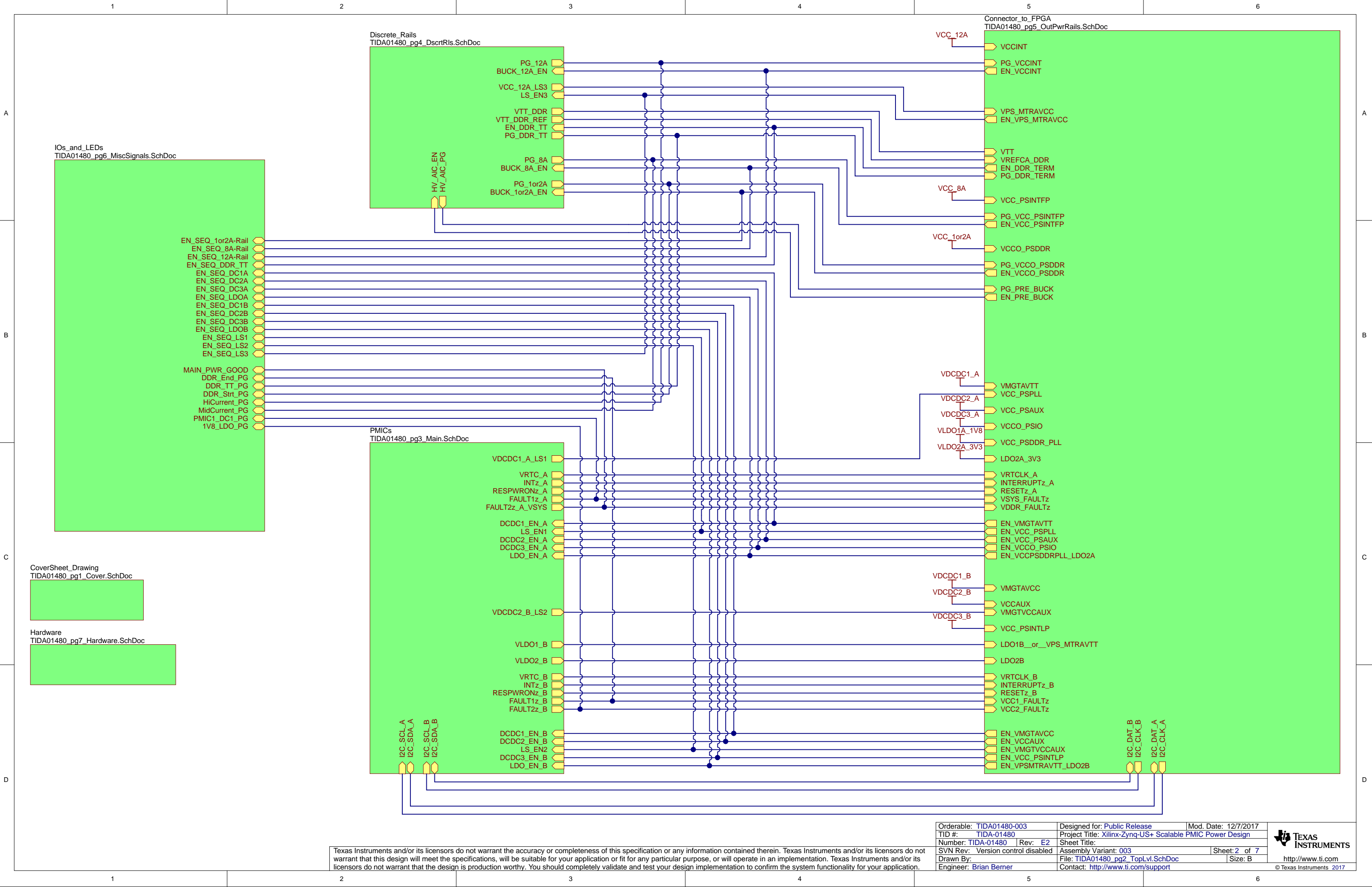
D



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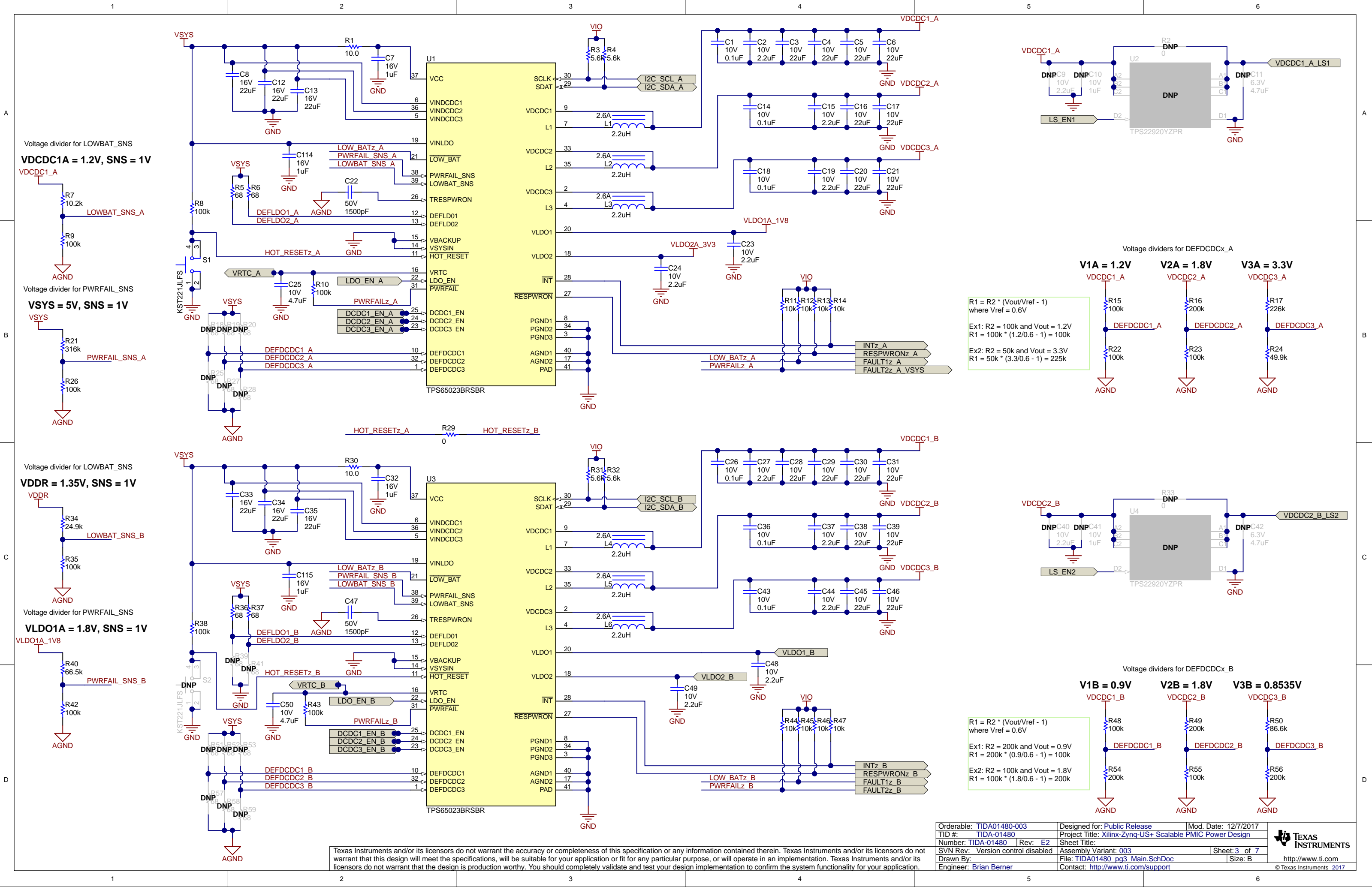
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TID #: TIDA-01480	Project Title: Xilinx-Zynq-US+ Scalable PMIC Power Design	Sheet Title:	
Number: TIDA-01480	Rev: E2	Assembly Variant: 003	
Drawn By:	File: TIDA01480_pg1_Cover.SchDoc	Size: B	
Engineer: Brian Berner	Contact: http://www.ti.com/support		



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Number: TIDA-01480	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 2 of 7
Drawn By:	File: TIDA01480_pg2_TopLvl.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	



Voltage divider for LOWBAT_SNS

VDCDC1A = 1.2V, SNS = 1V

Voltage divider for PWRFAIL_SNS

VSYS = 5V, SNS = 1V

Voltage divider for LOWBAT_SNS

VDDR = 1.35V, SNS = 1V

Voltage divider for PWRFAIL_SNS

VLDO1A = 1.8V, SNS = 1V

$R1 = R2 * (Vout/Vref - 1)$
where $Vref = 0.6V$

Ex1: $R2 = 100k$ and $Vout = 1.2V$
 $R1 = 100k * (1.2/0.6 - 1) = 100k$

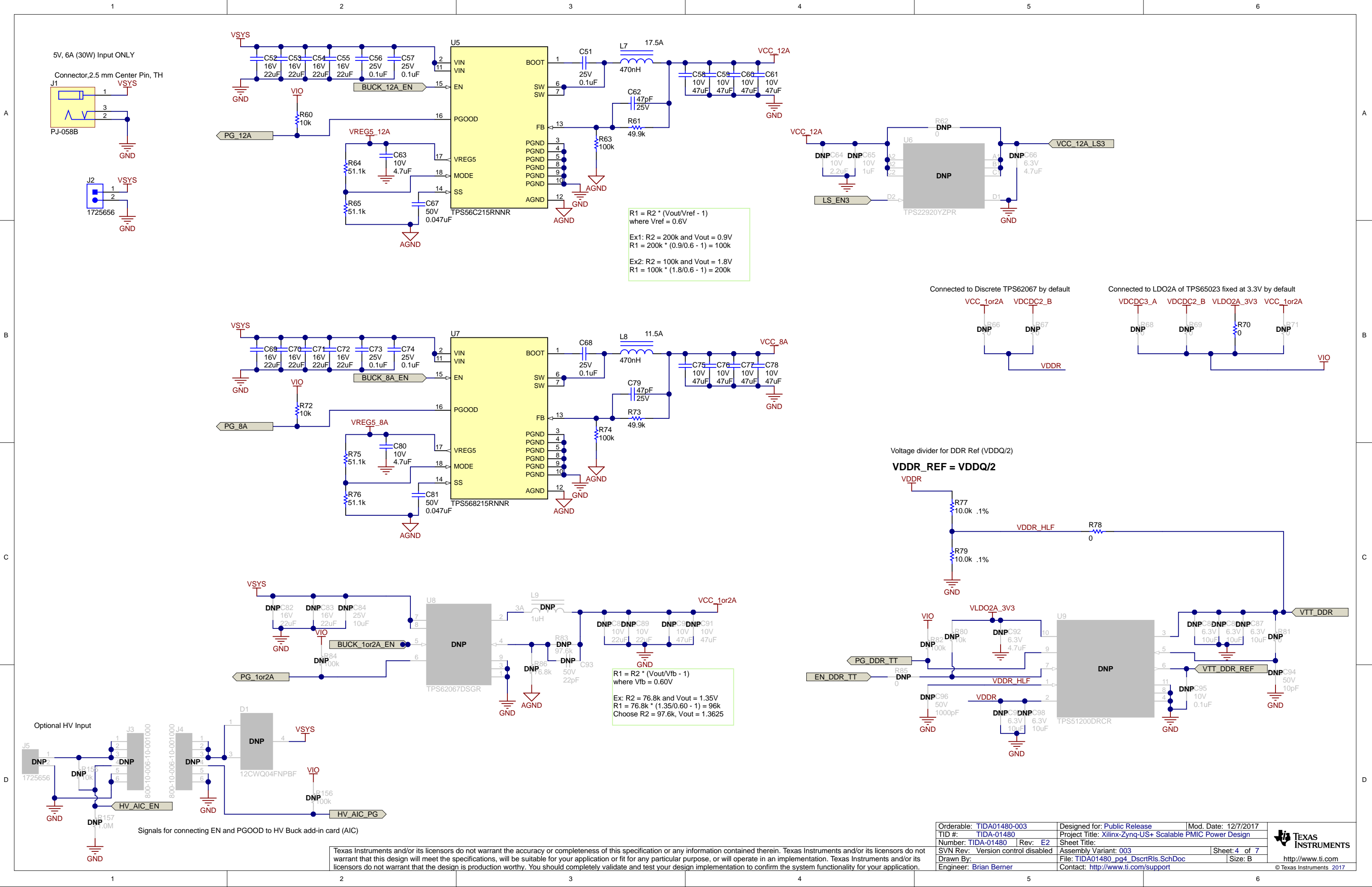
Ex2: $R2 = 50k$ and $Vout = 3.3V$
 $R1 = 50k * (3.3/0.6 - 1) = 225k$

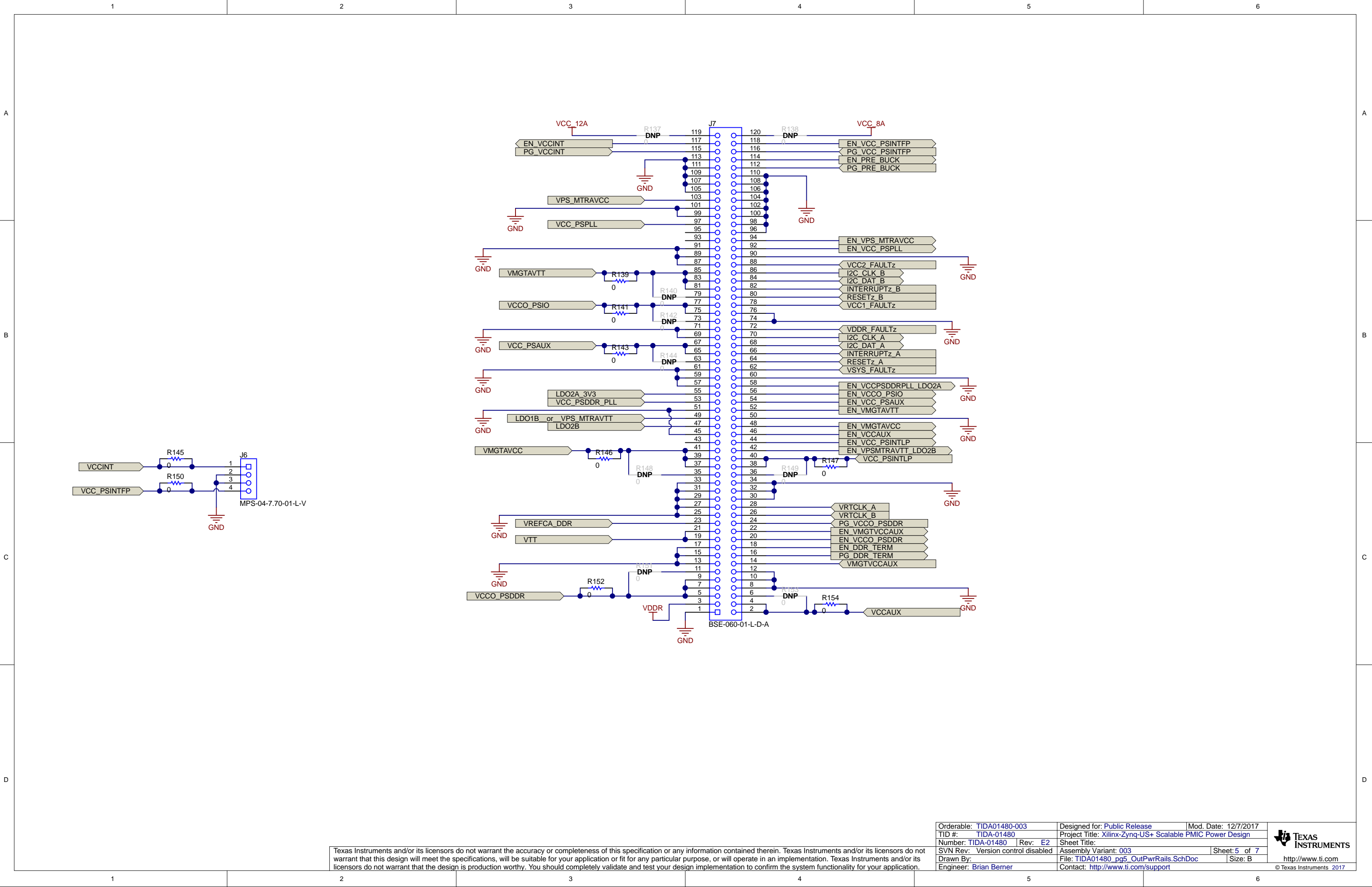
$R1 = R2 * (Vout/Vref - 1)$
where $Vref = 0.6V$

Ex1: $R2 = 200k$ and $Vout = 0.9V$
 $R1 = 200k * (0.9/0.6 - 1) = 100k$

Ex2: $R2 = 100k$ and $Vout = 1.8V$
 $R1 = 100k * (1.8/0.6 - 1) = 200k$

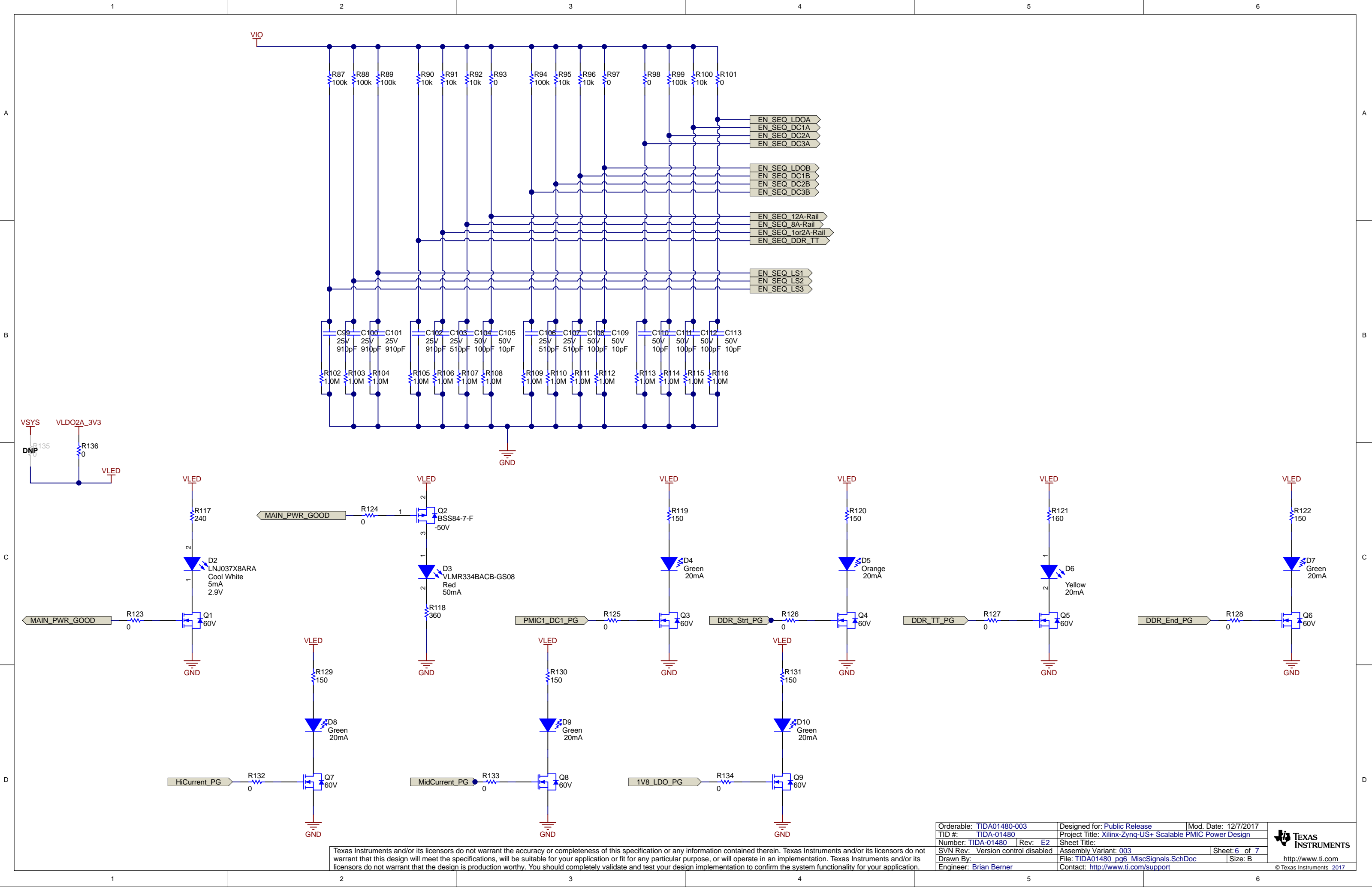
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SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 5 of 7
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Number: TIDA-01480	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 003	Sheet: 6 of 7
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